1. A method for the planarization of an integrated circuit structure comprising;

providing a substrate having a plurality of patterned regions;

polishing said substrate with an initial chemical mechanical polishing slurry until partial planarization occurs; and

continuing to final planarization with a second slurry.

2. The method of claim 1 wherein said integrated circuit structure comprises shallow trench isolation.

3. The method of claim 2 wherein said shallow trench isolation comprises silicon oxide, silicon nitride and polysilicon layers in various configurations.

4. The method of claim 1 wherein said initial slurry comprises silica-based slurry whose compositions ranges from 10 wt. % to 20 wt.% silica.

5. The method of claim 1 wherein said initial slurry comprises a diluted ceria-based slurry with the compositions that ranges from 0.5 wt. % to 1.0 wt % ceria.

6. The method of claim 1 wherein said polishing said substrate with said initial

chemical mechanical polishing slurry until partial planarization occurs comprises a control of polishing time so as to avoid overpolishing of a stop layer.

7.The method of claim 1 wherein said second slurry consists of a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria.

8. The method of claim 1 wherein said continuing to final planarization with said second slurry completes said planarization.

9. A method for the planarization of an integrated circuit structure comprising;

providing a substrate having a plurality of patterned regions wherein said substrate is to be planarized to a stop layer;

polishing said substrate with a first chemical mechanical polishing slurry composition until partial planarization occurs; and

thereafter continuing to final planarization with a second slurry.

10. The method of claim 9 wherein said integrated circuit structure comprises shallow trench isolation comprising silicon oxide and wherein said stop layer comprises one or more silicon nitride or polysilicon layers.

11. The method of claim 9 wherein said first slurry comprises a diluted ceria-based slurry with compositions ranging from 0.5 wt. % to 1.0 wt % ceria.

12. The method of claim 9 wherein said first slurry comprises silica-based slurry whose compositions ranges from 10 wt. % to 20 wt.% silica.

13. The method of claim 9 wherein said polishing said substrate with said first chemical mechanical polishing slurry composition until partial planarization occurs further comprises a control of polishing time so as to avoid overpolishing of said stop layer.

14. The method of claim 9 wherein said second slurry consists of a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria.

15. A method for the planarization of an integrated circuit structure comprising

providing a substrate having a plurality of patterned regions wherein said substrate is to be planarized to a stop layer;

polishing said substrate with a diluted chemical mechanical polishing slurry composition and controlling polishing time so that said stop layer is not exposed; and

thereafter continuing to final planarization to said stop layer with a more concentrated composition of said chemical mechanical polishing slurry.

16. The method of claim 15 wherein the integrated circuit structure comprises shallow trench isolation.

17. The method of claim 16 wherein said shallow trench isolation comprises silicon oxide and wherein said stop layer comprises one or more silicon nitride or polysilicon layers.

18. The method of claim 15 wherein said diluted slurry comprises a diluted ceria-based slurry with compositions ranging from 0.5 wt. % to 1.0 wt % ceria.

19. The method of claim 15 wherein said more concentrated slurry composition consists of a ceria-based slurry with composition ranging from 1.0 wt. % to 2.0 wt. % ceria.